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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,076	10/04/2003	Paul E. McKenney	BEA920030004US1	3528

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EXAMINER	
BERTRAM; RYAN	
ART UNIT	**PAPER NUMBER**
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/679,076	MCKENNEY ET AL.	
	Examiner	Art Unit	
	Ryan Bertram	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges receipt of amendment in response to the office action dated 10/04/2006, which amendment was received 01/02/2007. At this point, claims 1-12, and 16- 20 have been amended. Claims 1-20 are now pending in the application.

I. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 18-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 18-20 refer to a computer readable medium which is disclosed in the specification as being a modulated carrier signal. Since a modulated carrier signal is neither tangible nor concrete, it is non-statutory. The examiner recommends changing the claim language in claim 18 to read "a recordable data storage medium...".

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Tremblay et al. (US 2004/0162967) hereafter Tremblay.

1. Regarding claim 1, Tremblay teaches a method comprising: utilizing a hardware approach to transactional memory to execute a code section relating to memory (see paragraph [0068]);

and, where utilizing the hardware approach to transactional memory fails a threshold in executing the code section, utilizing a software approach to locking memory to execute the code section relating to the memory (see paragraph [0070]).

2. Regarding claim 2, Tremblay teaches the method of claim 1, further comprising utilizing the software approach to locking memory to execute other code sections relating to the memory (see paragraph [0070]).

3. Regarding claims 3 and 4, Tremblay teaches the method of claim 1, wherein utilizing the hardware approach to transactional memory to execute the code section comprises: starting a transaction inclusive of the code section; and, conditionally executing the transaction; and the method of claim 3, wherein utilizing the hardware approach to transactional memory to execute the code section further comprises, upon

successfully completing the transaction, committing execution of the transaction to the memory to which the code section relates (see paragraphs [0064] and [0067]).

4. Regarding claims 5 and 6, Tremblay teaches the method of claim 1, wherein utilization of the hardware approach to transactional memory failing the threshold in executing the code section comprises the hardware approach to transactional memory aborting execution of the code section a single time; and the method of claim 1, wherein utilization of the hardware approach to transactional memory failing the threshold in executing the code section comprises the hardware approach to transactional memory aborting execution of the code section a predetermined plurality of times (see paragraphs [0070] and [0095]).

5. Regarding claim 8, Tremblay teaches the method of claim 1, wherein utilization of the hardware approach to transactional memory failing the threshold in executing the code section comprises utilizing information passed from a compiler to determine whether to utilize the software approach to locking memory to execute the code section (see paragraph [0065]).

6. Regarding claim 10, Tremblay teaches the method of claim 1, wherein utilizing the software approach to locking memory to execute the code section comprises: placing a lock on the memory to which the code section relates; executing the code section; committing execution of the code section to the memory as the code section is

executed; and, removing the lock on the memory to which the code section relates (see paragraph [0070]).

Claims 1-6, 8-10, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Rajwar et al. (US. 7,120,762) hereinafter Rajwar.

7. Regarding claim 1, Rajwar teaches a method comprising:

executing a code section relating to memory using a hardware approach to transactional memory **[see Col. 2, lines 30-36]**, and

where the hardware approach to transactional memory fails a threshold in executing the code section, executing the code section relating to the memory using a software approach to locking memory **[see Col. 3, lines 60-64]**

8. Regarding claim 2, Rajwar teaches the method of claim 1, further comprising executing other code sections relating to the memory using the software approach to locking memory **[see Col. 3, lines 60-64]**.

9. Regarding claim 3, Rajwar teaches the method of claim 1, wherein executing the code section relating to the memory using the hardware approach to transactional memory comprises

starting a transaction inclusive of the code section **[see Col. 2, lines 30-36]**; and,

conditionally executing the transaction **[see Col. 7, lines 44-50]**.

10. Regarding claim 4, Rajwar teaches the method of claim 3, wherein executing the code section relating to the memory using the hardware approach to transactional memory section further comprises, upon successfully completing the transaction, committing execution of the transaction to the memory to which the code section relates **[see Col. 2, lines 30-36]**.

11. Regarding claims 5 and 6, Rajwar teaches the method of claim 1, wherein the hardware approach to transactional memory failing the threshold in executing the code section comprises the hardware approach to transactional memory aborting execution of the code section a single time or a predetermined number of times **[see Col. 3, lines 60-64, the retry limit can be set at any number]**.

12. Regarding claim 8, Rajwar teaches the method of claim 1, wherein the hardware approach to transactional memory failing the threshold in executing the code section comprises utilizing information passed from a compiler to determine whether to utilize the software approach to locking memory to execute the code section **[see Col. 3, lines 1-5]**.

13. Regarding claim 9, Rajwar teaches the method of claim 1, wherein the hardware approach to transactional memory failing the threshold in executing the code section

comprises tracking a success rate of the hardware approach to transactional memory in executing the code section to determine whether to utilize the software approach to locking memory to execute the code section **[see Col. 8, lines 12-15]**.

14. Regarding claim 10, Rajwar teaches the method of claim 1, wherein executing the code section relating to the memory using the software approach to locking memory comprises:

placing a lock on the memory to which the code section relates **[see Fig 2, 30]**;

executing the code section **[see Fig. 2, 44]** ;

committing execution of the code section to the memory as the code section is executed; and **[see Fig. 2, 44]**,

removing the lock on the memory to which the code section relates **[see Fig. 2, 32]**.

15. Regarding claim 18, Rajwar teaches an article of manufacture comprising:

a tangible computer-readable medium **[see Fig. 1, 17]**; and,

means in the medium for executing a code section using a software approach to locking memory where a hardware approach to transactional memory has failed a threshold in executing the code section **[see Col. 2, lines 30-36; Col. 3, lines 60-64]**.

16. Regarding claim 19, Rajwar teaches the article of claim 18, wherein the means executes the code section using the software approach to locking memory where the

hardware approach to transactional memory has failed to execute the code section a predetermined one or more times **[see Col. 3, lines 60-64]**.

17. Regarding claim 20, Rajwar teaches the article of claim 18, wherein the tangible computer-readable medium is a recordable data storage medium **[see Fig. 1, 17]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay in view of Rajwar et al. (US 2003/0079094) hereafter Rajwar.

18. Regarding claim 9, Tremblay teaches all of the limitations of claim 1, as well as tracking a success rate of the hardware approach to transactional memory (see paragraph [0097]). However, he does not disclose using this rate to determine whether the software approach to locking memory should be used.

Rajwar teaches a method for speculatively executing critical sections of multi-threaded programs. He discloses using a table with values of historical success of previous execution of certain critical sections (see paragraph [0055]) in order to prevent using a hardware approach to execution if the critical sections will be more likely to be contested with (see paragraph [0021]).

Tremblay and Rajwar are analogous art because they are from the same field of endeavor of using software locks to execute a critical section of code.

Therefore, it would have been obvious to one have ordinary skill in the art at the time of invention to modify the tracking of a success rate of a hardware approach of code execution taught by Tremblay with the utilization of that success rate as taught by Rajwar in order to prevent using a hardware approach to execution if it is highly likely it will fail.

Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay in view of McKenney (US 2002/0078284).

19. Regarding claims 7 and 11, Tremblay teaches all of the limitations of claim 1, however he does not disclose that the utilization of the software approach to locking memory to execute the code section comprises utilizing one of a queued lock, a non-uniform memory architecture (NUMA) lock, and a reader-writer lock. Nor does he disclose utilizing a digital filter to as the threshold in determining whether to utilize the software approach to locking memory.

McKenney teaches a method for dynamically selecting an optimal lock mode in a multiprocessor environment. McKenney discloses the lock mode in NUMA machines consisting of a reader-writer lock mode, and an exclusive lock mode, which can includes queued locks (see col. 3, lines8-10, and col. 4, lines 10-13), to ensure process synchronization (see col. 2, lines 3-7). He also discloses using a digital filter for taking measurements to determine an optimal opportunity for switching to an alternative locking mode (see paragraph col. 9, lines 51-66).

Tremblay and McKenney are analogous art because they are from the same field of endeavor of using software locks to execute a critical section of code.

Therefore, it would have been obvious to one have ordinary skill in the art at the time of invention to modify the software approach to locking memory taught by Tremblay with the specific lock types taught by McKenney in order for an operating system to operate more efficiently, and to determine the optimal opportunity for switching to an alternative locking mode.

Claims 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay in view of Radovic et al. (US 2004/0098723) hereafter Radovic.

20. Regarding claims 12-17, Tremblay teaches a system comprising a processor having transactional memory capability (see claim 13). He also teaches a system comprising a plurality of nodes interconnected to one another, one of the plurality of nodes inclusive of the processor and the memory (see paragraph [0053-0054]). Tremblay further teaches utilizing a software approach to locking memory where the transactional memory capability has initially failed a threshold in executing a code section (see paragraphs [0068] and [0070]). However, Tremblay does not disclose the system having memory storing a spin lock/unlock function to execute a code section, nor does he disclose the memory further storing the code section, the code section programmed to call the spin lock function to execute, the spin lock function locking a portion of the memory to which the code section relates.

Radovic teaches a multiprocessing system employing various implementations of software locks. He discloses that the sets of instructions for executing the spin lock/unlock functions may be stored in any type of computer memory in order to provide internode coherency within a multiprocessor system (see paragraph [0026]).

Tremblay and Radovic are analogous art because they are from the same field of endeavor of using software locks to execute a critical section of code.

Therefore, it would have been obvious to one have ordinary skill in the art at the time of invention to modify the processor having transactional memory capability and the means for locking memory taught by Tremblay with the computer memory capable of storing code with these means taught by Radovic in order for a multiprocessor system to maintain internode coherency.

Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay in view of Rubinstein (US 5,913,215).

21. Claims 18-20 are method versions of claims 1 and 6, enabled by instructions rather than hardware. Tremblay discloses an apparatus for performing the method of claims 18-20, as discussed above in the rejection of claims 1 and 6.

Tremblay, however, does not expressly disclose that the method is performed by a software series of instructions, instead disclosing a set of hardware components. Rubinstein discloses, on Col. 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

Tremblay and Rubinstein are analogous art because they are from the same general field of endeavor, namely computer-controlled methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the apparatus of Tremblay by embodying it in executable instructions.

The motivation for doing so is portability and ease of installation. For example, it is well known that a method encoded in a program may be installed onto different systems much more quickly and easily than can hardware components designed to perform the same method.

Therefore, it would have been obvious to combine Tremblay with Rubinstein for the benefits shown above, to obtain the invention as specified in claims 18-20.

Claims 12-17 and 11are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar in view of Radovic et al (US 2004/0098723) hereinafter Radovic.

22. Regarding claim 12, Rajwar teaches a system comprising:

a processor having transactional memory capability **[see Fig. 1, 16]**; and,

a memory storing a lock function to execute a code section via a software approach to locking memory where the transactional memory capability has initially failed a threshold in executing the code section **[see Fig. 1, 17; Col. 2, lines 30-36; Col. 3, lines 60-64]**.

Rajwar does not disclose expressly that the locking function is a spin lock function.

Radovic discloses a multiprocessing system that employs a variety of software locks, including one of a spin lock **[see paragraph 0008]**.

Rajwar and Radovic are analogous art because they are from the same field of endeavor of using software locks to execute critical sections of code.

At the time of invention it would have been obvious to one having ordinary skill in the art to modify Rajwar's system of employing software locks with the spin lock taught by Radovic.

The motivation for doing so would have been to ensure that only one process at a time could access a critical section of memory **[see Radovic, paragraph 0008]**.

Therefore it would have been obvious to combine Radovic with Rajwar for the benefit of preventing multiple process accesses to a critical section of memory to obtain the invention as specified in claims 12-17.

23. Regarding claim 13, Rajwar and Radovic teach the system of claim 12, further comprising a plurality of nodes interconnected to one another, one of the plurality of nodes inclusive of the processor and the memory **[see Rajwar, Fig. 1]**.

24. Regarding claim 14, Rajwar and Radovic teach the system of claim 12, wherein the memory further stores the code section, the code section programmed to call the spin lock function to execute, the spin lock function locking a portion of the memory to which the code section relates **[see Radovic, paragraph 0026]**.

25. Regarding claim 15, Rajwar and Radovic teach the system of claim 14, wherein the memory further stores a spin unlock function that the code section calls to unlock the portion of the memory to which the code section relates **[see Radovic, paragraph 0026]**.

26. Regarding claim 16, Rajwar and Radovic teach the system of claim 14, wherein the spin lock function initially uses the transactional memory capability in locking the portion of the memory to which the code section relates, and falls back to the software approach to locking memory upon the transactional memory capability failing the threshold in executing the code section **[see Rajwar, Col. 2, lines 30-36; Col. 3, lines 60-64]**.

27. Regarding claim 17, Rajwar and Radovic teach the system of claim 12, wherein the software approach is used to execute the code section where the transactional memory capability has failed to execute the code section a predetermined one or more times **[see Rajwar, Col. 3, lines 60-64]**.

Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar in view of McKenney (US 2002/0078284).

28. Regarding claim 7, Rajwar teaches the method of claim 1, wherein utilization of the hardware approach to transactional memory failing the threshold in executing the code section comprises using a success rate in determining whether to utilize the software approach to locking memory to execute the code section **[see above]**.

Rajwar does disclose expressly that a digital filter is used as the threshold for determining whether to use the software approach.

McKenney discloses a method for dynamically selecting an optimal lock mode in a multiprocessor environment. He also discloses using a digital filter for taking measurements to determine an optimal opportunity for switching to an alternative locking mode **[see paragraph col. 9, lines 51-66]**.

Rajwar and McKenney are analogous art because they are from the same field of endeavor of using software locks to execute critical sections of code.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system of Rajwar with the digital filter taught by McKenney.

The motivation for doing so would have been to determine the optimal opportunity for switching to an alternative locking mode **[see McKenney, Paragraph 29]**.

Therefore, it would have been obvious to combine Rajwar with Radovic for the benefit of efficiently determining when to switch to a different locking mode to obtain the invention as specified in claim 7.

29. Regarding claim 11, Rajwar teaches the method of claim 1 as described above.

Rajwar does not disclose that executing the code section relating to the memory using the software approach to locking memory comprises utilizing one of a queued lock, a non-uniform memory architecture (NUMA) lock, and a reader-writer lock.

McKenney discloses the lock mode in NUMA machines consisting of a reader-writer lock mode, and an exclusive lock mode, which can includes queued locks **[see col. 3, lines8-10, and col. 4, lines 10-13]**, to ensure process synchronization.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system of Rajwar with software locking options taught by McKenney.

The motivation for doing so would have been to operate an operating system more efficiently **[see McKenney, Paragraph 29]**.

Therefore, it would have been obvious to combine Rajwar with Radovic for the benefit of a more efficient operating system to obtain the invention as specified in claim.

III. RESPONSE TO APPLICANT'S 131 AFFADAVIT

The affidavit filed on 01/02/2007 under 37 CFR 1.131 has been considered but is ineffective to overcome the Tremblay reference.

The Tremblay reference is a U.S. patent or U.S. patent application publication of a pending or patented application that claims the rejected invention. An affidavit or declaration is inappropriate under 37 CFR 1.131(a) when the reference is claiming the same patentable invention, see MPEP § 2306. If the reference and this application are not commonly owned, the reference can only be overcome by establishing priority of invention through interference proceedings. See MPEP Chapter 2300 for information on initiating interference proceedings. If the reference and this application are commonly owned, the reference may be disqualified as prior art by an affidavit or declaration under 37 CFR 1.130. See MPEP § 718.

IV. RESPONSE TO APPLICANT'S ARGUMENTS

Regarding applicant's traversal of the rejection of claims 1-17, the examiner directs the applicant's attention to **PART III** of the instant office action.

Applicant's arguments with respect to claims 18-20 have been considered but are moot in view of the new ground(s) of rejection.

V. CLOSING COMMENTS

Conclusion

(a) **Status of Claims In the Application**

(i) Claims Rejected In the Application

Per the instant office action, claims 1-20 have received a second action on the merits and are subject of a second action non-final.

(b) **Directions of Future Correspondences**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Bertram whose telephone number is 571-270-1377. The examiner can normally be reached on Mon-Fri 8am-5pm ET (Alternate Fridays off).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RDB

DONALD SPARKS
SUPERVISORY PATENT EXAMINER